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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/063,880	05/21/2002	Kuo-Ming Chen	NAUP0481USA	2347

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EXAMINER	
NGUYEN, DILINH P	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 11/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/063,880	CHEN, KUO-MING	
	Examin r	Art Unit	
	DiLinh Nguyen	2814	

-- Th MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 September 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26 and 28-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26 and 28-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

Claim 8 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

The independent claim 1 comprises the limitation of claim 8.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 6-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Nishiyama (U.S. Pat. 6107685).

Nishiyama discloses a semiconductor package (figs. 3D and 4) comprising:

a substrate 25/33;

a plurality of first solder pads positioned on a surface of the substrate, each of the first solder pads having a first diameter; and

at least a second solder pad 34 positioned on a corner region of the substrate surface (figs. 3D and 4), the second solder pad having a second diameter greater than the first diameter. Since Nishiyama discloses all claimed structure features. Therefore,

the package inherently sustains a stronger thermal stress and a stronger fatigue strength.

- Regarding claim 6, since Nishiyama discloses all claimed structure features. Therefore, the package inherently discloses the predetermined region comprises a high stress region.
- Regarding claim 7, Nishiyama discloses the first solder pads are arranged in a matrix at a center region of the substrate.
- Regarding claim 8, Nishiyama discloses the corner region comprises the corners of the substrate.

3. Claims 1 and 5-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Juso et al. (U.S. Pat. 6265783).

Juso et al. disclose a semiconductor package (figs. 2 and 4) comprising:

a substrate;

a plurality of first solder pads 9 positioned on a surface of the substrate, each of the first solder pads having a first diameter; and

at least a second solder pad 4 positioned on a corner region of the substrate surface (fig. 2 and 4), the second solder pad having a second diameter greater than the first diameter. Since Juso et al. disclose all claimed structure features. Therefore, the package inherently sustains a stronger thermal stress and a stronger fatigue strength.

- Regarding claim 5, Juso et al. disclose the substrate comprises a chip 1.

- Regarding claim 6, since Juso et al. disclose all claimed structure features. Therefore, the package inherently discloses the predetermined region comprises a high stress region.
- Regarding claim 7, Juso et al. disclose the first solder pads are arranged in a matrix at a center region of the substrate.
- Regarding claim 8, Juso et al. disclose the corner region comprises the corners of the substrate.

4. Claims 1 and 5-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Lin et al. (U.S. Pat. 5216278).

Lin et al. disclose a semiconductor package (fig. 1) comprising:

a substrate 12;

a plurality of first solder pads 34 positioned on a surface of the substrate, each of the first solder pads having a first diameter; and

at least a second solder pad 34 positioned on a corner region of the substrate surface, the second solder pad having a second diameter greater than the first diameter. Since Lin et al. disclose all claimed structure features. Therefore, the package inherently sustains a stronger thermal stress and a stronger fatigue strength.

- Regarding claim 5, Lin et al. disclose the substrate comprises a chip 18.
- Regarding claim 6, since Lin et al. disclose all claimed structure features. Therefore, the package inherently discloses the predetermined region comprises a high stress region.

- Regarding claim 7, Lin et al. disclose the first solder pads are arranged in a matrix at a center region of the substrate.
- Regarding claim 8, Lin et al. disclose the corner region comprises the corners of the substrate.

5. Claims 1, 5-8 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Kumazawa et al. (U.S. Pat. 5569960).

Kumazawa et al. disclose a semiconductor package (fig. 1, column 7, lines 12 et seq.) comprising:

a substrate 3;

a plurality of first solder pads 6a/6b/6c positioned on a surface of the substrate, each of the first solder pads having a first diameter; and

at least a second solder pad 6d positioned on a corner region of the substrate surface (fig. 2, column 6, lines 30-35), the second solder pad having a second diameter greater than the first diameter (fig. 1, column 7, lines 35-37). Since Kumazawa et al. disclose all claimed structure features. Therefore, the package inherently sustains a stronger thermal stress and a stronger fatigue strength.

- Regarding claim 5, Kumazawa et al. disclose the substrate comprises a chip 1.
- Regarding claim 6, since Kumazawa et al. disclose all claimed structure features. Therefore, the package inherently discloses the predetermined region comprises a high stress region.
- Regarding claim 7, Kumazawa et al. disclose the first solder pads are arranged in a matrix at a center region of the substrate.

- Regarding claim 8, Kumazawa et al. disclose the corner region comprises the corners of the substrate.
- Regarding claim 16, Kumazawa et al. disclose the first and second solder pads 6 comprise a solder ball pad 7 connecting to a solder ball 8 and using the solder ball to connect to a circuit board 9.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 2-4 and 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over (Kumazawa et al. or Lin et al.) in view of Applicant Admitted Prior Art (figs. 1 and 4).

- Regarding claim 9, Kumazawa et al. disclose the claimed invention except for not specifically point out that the predetermined region comprises the circumferences of a plurality of concentric circles on the substrate.

AAPA (fig. 4) disclose a plurality of first solder pads 14 and a plurality of second solder pads 24, the plurality of second solder pads 24 positioned on a predetermined region; wherein the predetermined region comprises the circumferences of a plurality of concentric circles on the substrate. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Kumazawa et al. to prevent the package not crack easily at the corner of the chip.

- Regarding claims 2-3, AAPA (fig. 1) disclose a substrate 18 comprises a plastic substrate or a ceramic substrate.
- Regarding claim 4, Kumazawa et al. disclose the substrate comprises a circuit substrate (column 9, lines 19-20).
- Regarding claim 10, AAPA discloses the second solder pads on each of the concentric circle circumferences are arranged with an equal interval.
- Regarding claim 11, AAPA discloses the predetermined region comprises the corners of the substrate on an outside portion of a maximum circle on the substrate.
- Regarding claim 12, AAPA discloses the predetermined region comprises the circumference of a maximum circle on the substrate.
- Regarding claim 13, AAPA discloses the predetermined region comprises at least a grounded solder pad.

3. Claims 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over (Kumazawa et al. or Lin et al.) in view of Pu et la. (U.S. Pat. 6350669).

Kumazawa et al. fail to disclose the first and second solder pads comprise a solder bump pad, the solder bump pad connecting to a solder bump and using the solder bump to connect to a chip.

Pu et al. disclose a semiconductor package (cover fig.) comprising:

a substrate 310;

a plurality of solder pads on a surface of the substrate and the solder pads comprises a solder bump pad, the solder bump pad connecting to a solder bump 321

and using the solder bump to connect to a chip 300. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Kumazawa et al. to prevent the collapsing of the BGA package against the circuit board.

- Regarding claim 15, it is obvious to have an underfill layer is filled in a gap between the chip and the substrate to reduce mismatch of a coefficient of thermal expansion of the die with the substrate.

4. Claims 17, 20-22 and 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pu et al. (U.S. Pat. 6350669) in view of Kumazawa et al. (U.S. Pat. 5569960).

Pu et al. discloses a semiconductor device (cover fig.) comprising:

a substrate 310;

a plurality of first solder bump pads A2 positioned on a first surface of the substrate, each of the first solder bump pads having a first diameter and

at least a second solder bump pad A1 positioned on a first predetermined region of the first surface, the second solder bump pad having a second diameter greater than the first diameter (column 4, lines 52-54), each of the first solder bump pads and the second solder bump pad being connected to a solder bump 321 that is connected to a chip 300.

Pu et al. fail to disclose a plurality of first solder ball pads positioned on a second surface of the substrate, each of the first solder ball pads having a third diameter, and at least a second solder ball pad positioned on a second predetermined region of the

second surface, the second solder ball pad having a second diameter greater than the third diameter.

Kumazawa et al. disclose a semiconductor device (figs. 1-2) comprising:

a plurality of first solder ball pads 6a/6b/6c positioned on a second surface of the substrate 3, each of the first solder ball pads having a third diameter; and

at least a second solder ball pad 6d positioned on a second predetermined region of the second surface, the second solder ball pad having a fourth diameter greater than the third diameter (column 7, lines 35-40), each of the first solder ball pads and the second solder ball pad being connected to a solder ball 8 that is connected a printed circuit board 9. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Pu et al. to provide a bump connection structure disposed at the outer peripheral edge of the substrate to provide a high reliability for the semiconductor package device, as shown by Kumazawa et al.

- Regarding claim 20, since Pu et al. in view of Kumazawa et al. discloses all claimed structural features. Therefore, the package inherently comprises a high stress region at the first predetermined region and the second predetermined region.
- Regarding claim 21, Pu et al. disclose the first solder bump pad are arranged in a matrix at a center region of the substrate.
- Regarding claim 28, Kumazawa et al. disclose the first solder ball pads are arranged in a matrix at a center region of the substrate (fig. 2).

- Regarding claims 22 and 29, Kumazawa et al. disclose the predetermined region comprises the corners on the surface of the substrate.

5. Claims 18-19 and 23-26 and 30-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Selna in view of Applicant Admitted Prior Art (figs. 1 and 4).

- Regarding claims 23 and 30, Kumazawa et al. disclose the claimed invention except for not specifically point out that the predetermined region comprises the circumferences of a plurality of concentric circles on the substrate.

AAPA (fig. 4) disclose a plurality of first pads 14 and a plurality of second pads 24, the plurality of second pads 24 positioned on a predetermined region; wherein the predetermined region comprises the circumferences of a plurality of concentric circles on the substrate. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Kumazawa et al. to prevent the package not crack easily at the corner of the chip.

- Regarding claims 18-19, AAPA (fig. 1) disclose a substrate 18 comprises a plastic substrate or a ceramic substrate.
- Regarding claims 24 and 31, AAPA discloses the second pads on each of the concentric circle circumferences are arranged with an equal interval.
- Regarding claims 25 and 32, AAPA discloses the predetermined region comprises the corners of the substrate on an outside portion of a maximum circle on the substrate.
- Regarding claims 26 and 33, AAPA discloses the predetermined region comprises the circumference of a maximum circle on the substrate.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DiLinh Nguyen whose telephone number is (703) 305-6983. The examiner can normally be reached on 8:00AM - 6:00PM (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

DLN
November 14, 2003

LONG PHAM
PRIMARY EXAMINER